

Three-Phase MOSFET Bridge, With Gate Driver and Optical Isolation

DESCRIPTION: A 100 VOLT, 60 AMP, THREE PHASE MOSFET BRIDGE

ELECTRICAL CHARACTERISTICS PER MOSFET DEVICE ($T_j=25^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MOSFET SPECIFICATIONS					
Drain to Source Breakdown Voltage $I_C = 250 \mu\text{A}, V_{GS} = 0\text{V}$	BV_{CSS}	100	-		V
Continuous Drain Current $T_C = 25^{\circ}\text{C}$ $T_C = 90^{\circ}\text{C}$	I_D	-	-	60 50	A
Pulsed Drain Current, 1mS	I_{DM}			100	A
Gate to Source Voltage	V_{GS}	-	-	+/-20	V
Gate-Source Leakage Current , $V_{GS} = +/-20\text{V}$	I_{GSS}			+/- 100	nA
Gate Threshold Voltage, $I_C=1\text{mA}$	$V_{GS(TH)}$	2		4	V
Zero Gate Voltage Drain Current $V_{CS} = 600 \text{V}, V_{GE}=0\text{V} T_i=25^{\circ}\text{C}$ $V_{CS} = 480 \text{V}, V_{GE}=0\text{V} T_i=125^{\circ}\text{C}$	I_{CSS}	-	-	250 500	μA μA
On-State Resistance, $T_C = 25^{\circ}\text{C}$ $I_D = 10\text{A}, V_{GS} = 15\text{V},$	R_{DSon}	-	0.012	0.015	V
Input Capacitance Output Capacitance Reverse Transfer Cap. $V_{CS} = 25 \text{V}, V_{GE} = 0 \text{V}, f = 1 \text{MHz}$	C_{iss} C_{oss} C_{res}		3950 850 250		pF
Maximum Thermal Resistance	$R_{\theta JC}$	-	-	0.7	$^{\circ}\text{C/W}$

SENSITRON SEMICONDUCTOR

TECHNICAL DATA

DATA SHEET 4096, Rev A

Gate Driver

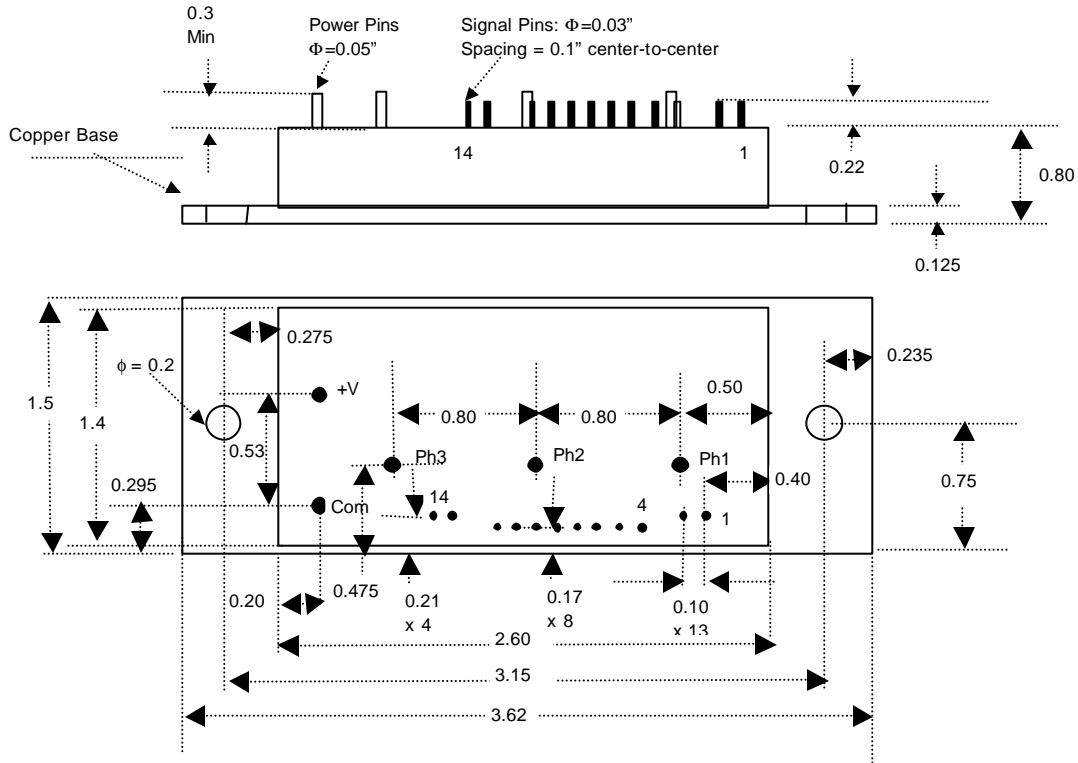
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	VCC	10	15	20	V
Input On Current	HIN, LIN	1.6	-	5	mA
Opto-Isolator Logic High Input Threshold	I_{th}		1.6		mA
Input Reverse Breakdown Voltage	BV_{in}	5			V
Input Forward Voltage @ $I_{in} = 5mA$	V_F		1.5	1.7	V
Under Voltage Lockout	VCCUV	7.0	-	9.7	V
ITRIP Threshold Voltage ⁽¹⁾	ITRIP _{th}	0.4	0.49	0.58	V
Turn On Delay	t_{ond}	-	-	1000	nsec
Turn On Rise Time	t_r	-	-	100	nsec
Turn Off Delay	t_{offd}	-	-	1300	nsec
Turn Off Fall Time	t_f	-	-	100	nsec
Input-Output Isolation Voltage		1000			V

Maximum operating Junction Temperature	T_{jmax}	-40	-	150	°C
Maximum Storage Junction Temperature	T_{jmax}	-55	-	150	°C

(1) Once ITRIP reaches threshold, the driver latches off. This condition can be reset by holding all three low-side inputs high for more than 10 μ sec or by recycling the V_{cc} supply.

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Package Drawing:



Package Material:

Base: Copper
Frame: Nickel
Lid: Plastic
Power Terminals: Copper

Signal Terminals & Truth Table:

HIN1,2,3	LIN1,2,3	HO1,2,3	LO1,2,3
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

Pin #	Function
1	+15V
2	PWR-GRND
3	NC
4	HIN1
5	HIN2
6	HIN3
7	SGN-GRND
8	LIN1
9	LIN2
10	LIN3
11	SGN-GRND
12	NC
13	ITRIP
14	ITRIP-RTN

Note: This device can be used with a non-inverting input logic, if LIN and HIN are swapped.

TECHNICAL DATA

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