TECHNICAL DATA
Datasheet 4118, Rev. D.1

Three-Phase MOSFET BRIDGE, With Gate Driver and Optical Isolation

DESCRIPTION: A 100 VOLT, 80 AMP, THREE PHASE MOSFET BRIDGE

ELECTRICAL CHARACTERISTICS PER MOSFET DEVICE (T_j=25^{0}C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MOSFET SPECIFICATIONS					
Drain-to-Source Breakdown Voltage I_D = 500 μA, V_{GS} = 0V	BV_{DSS}	100	-	-	V
Continuous Drain Current T_C = 25 ^{O}C T_C = 90 ^{O}C	I_D	-	-	80 70	A
Pulsed Drain Current, Pulse Width limited to 1 msec	I_{DM}	-	-	200	A
Zero Gate Voltage Drain Current V_{DS} = 100 V, V_{GS}=0V T_i=25^{o}C V_{DS}= 80 V, V_{GS}=0V T_i=125^{o}C	I_{CSS}	-	-	 1 3	 mA mA
Static Drain-to-Source On Resistance, T_j = 25 ^{O}C T_j = 150 ^{O}C I_D= 60A, V_{GS} = 15V,	R_{DSon}	-	0.009 0.018	0.012 -	Ω
Maximum Thermal Resistance	$R_{\theta JC}$	-	-	0.65	^{o}C/W
Maximum operating Junction Temperature	T_{jmax}	-40	-	150	^{o}C
Maximum Storage Junction Temperature	T_{jmax}	-55	-	150	^{o}C

TECHNICAL DATA
Datasheet 4118, Rev. D.1

PRODUCT PARAMETERS - (T_C=25 °C unless otherwise noted)

Over-Temperature Shutdown					
Over-Temperature Shutdown	Tsd	100	105	110	°C
Over-Temperature Output	Tso		10		10mV/°C
Over-Temperature Shutdown Hysteresis			20		°C

DIODES CHARACTERISTICS					
Continuous Source Current, T_C = 90 °C	I_S	-	-	70	A
Diode Forward Voltage, I_S = 60A, T_j = 25 °C	V_{SD}	-		1.15	V
Diode Reverse Recovery Time (I_S=50A, V_{DD}=50V , di/dt=100 A/μs)	t_{rr}	-	70	-	nsec
Gate Driver					
Supply Voltage	VCC	14	15	18	V
Supply Input Current at Vcc, Pin 19, Without PWM Switching , with 10KHz PWM at Two Inputs			 35 50		 mA
Input On Current	HIN, LIN	2		5.0	mA
Opto-Isolator Logic High Input Threshold	I_{th}	-	1.6	-	mA
Input Reverse Breakdown Voltage	BV_{in}	5.0	-	-	V
Input Forward Voltage @ I_{in} = 5mA	V_F	-	1.5	1.7	V

Under Voltage Lockout	VCCUV	9.0	10.0	11.5	V
ITRIP Reference Voltage (1)	Itrip-ref	1.57	1.63	1.68	V
Input-to-Output Turn On Delay Output Turn On Rise Time Input-to-Output Turn Off Delay Output Turn Off Fall Time @ VCC=50V, ID=50A, T_C = 25	t_{ond} t_r t_{offd} t_f	- - - -	700 50 750 60	- - - -	nsec
Dead Time Requirement, for Shoot Through Prevention		600	750		nsec
Opto-Isolator Input-to-Output Isolation Voltage, momentary	-	-	2500	-	V
Opto-Isolator Operating Input Common Mode Voltage				1000	V
Opto-Isolator Operating Input Common Mode Transient Immunity, with Iin > 5mA				10	KV/usec
Pin-To-Case Isolation Voltage, DC Voltage		-	1500	-	V

DC Bus Current Sensor					
Shunt Resistor Value	-	-	5	-	mOhm
Current Amplifier Gain, Referenced to Signal Gnd			0.049		V/A
Current Amplifier DC Offset (Zero DC Bus Current)			0.010	0.030	V
Current Amplifier Response Time			3		usec

(1) ITRIP current limit is internally set to 35A peak. The set point can be lowered by connecting a resistor between Itrip-ref and Gnd. The set point can be increased by connecting a resistor between Itrip-ref and +5V ref. The off time duration is about 70 usec.

TECHNICAL DATA
Datasheet 4118, Rev. D.1

Figure 2 - Package Drawing Top & Side Views
(All dimensions are in inches, tolerance is +/- 0.010")

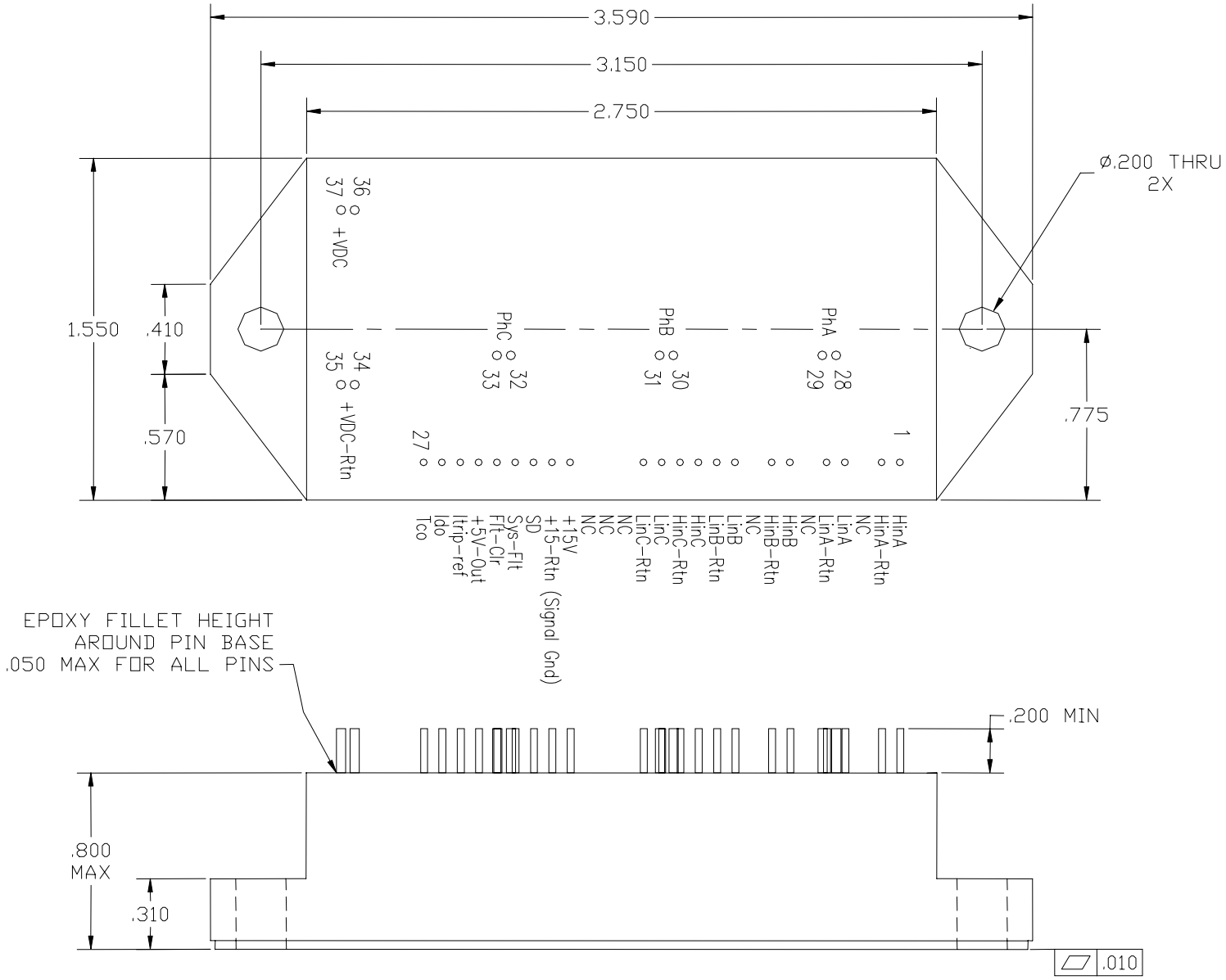
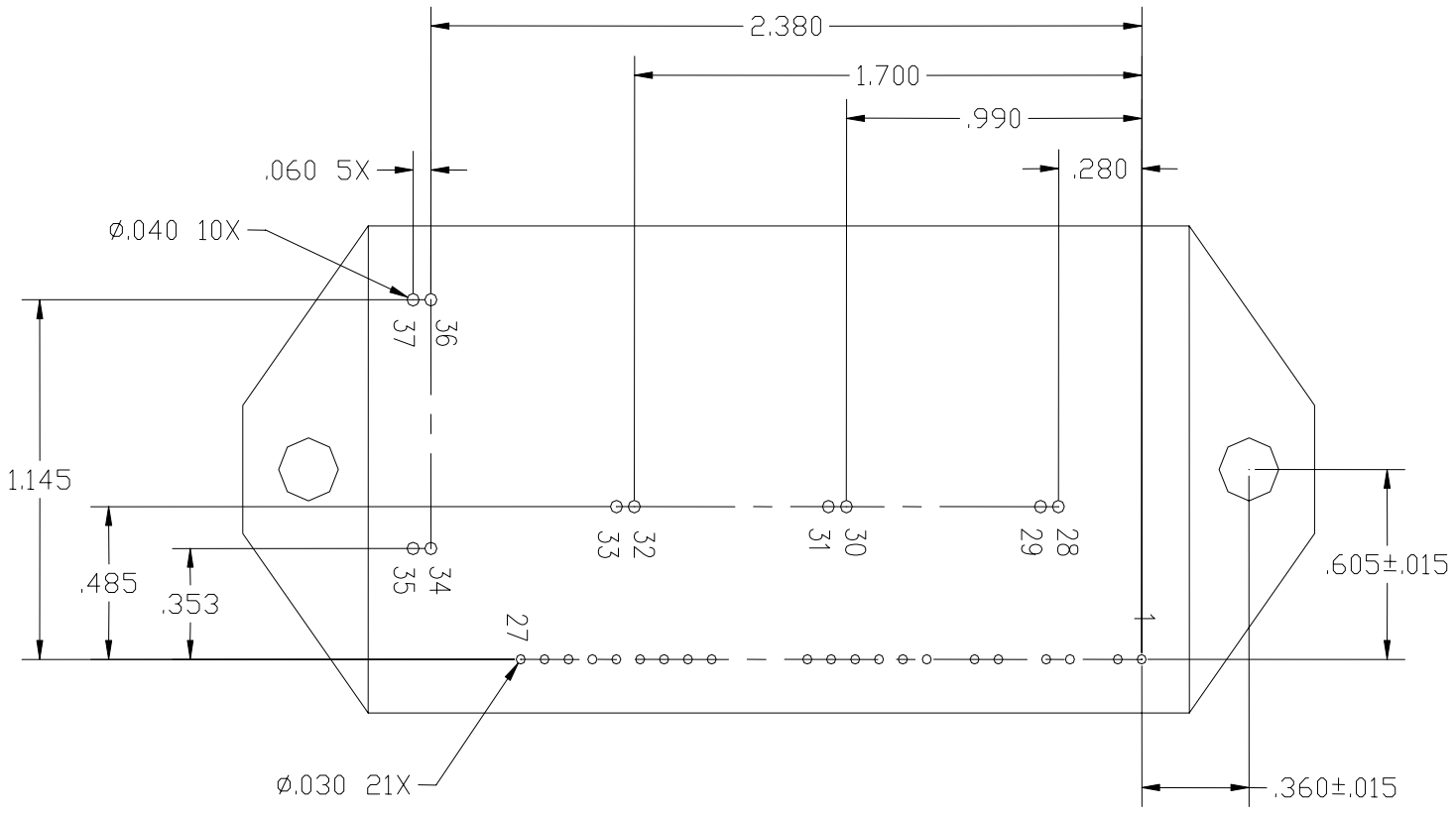


Figure 3 - Package Pin Locations
(All dimensions are in inches; tolerance is +/- 0.005" unless otherwise specified)



TECHNICAL DATA
Datasheet 4118, Rev. D.1

PIN OUT

Pin #	Name	Description
1	HinA	Isolated Drive Input for High-side MOSFET of Phase A
2	HinA-Rtn	Return for Input at 1
3	NC	Not Connected
4	LinA	Isolated Drive Input for Low-side MOSFET of Phase A
5	LinA-Rtn	Return for Input at 4
6	NC	Not Connected
7	HinB	Isolated Drive Input for High-side MOSFET of Phase B
8	HinB-Rtn	Return for Input at 7
9	NC	Not Connected
10	LinB	Isolated Drive Input for Low-side MOSFET of Phase B
11	LinB-Rtn	Return for Input at 10
12	HinC	Isolated Drive Input for High-side MOSFET of Phase C
13	HinC-Rtn	Return for Input at 12
14	LinC	Isolated Drive Input for Low-side MOSFET of Phase C
15	LinC-Rtn	Return for Input at 14
16	NC	Not Connected
17	NC	Not Connected
18	NC	Not Connected
19	Vcc	+15V input biasing supply connection for the controller. Under-voltage lockout keeps all outputs off for Vcc below 10.5V. Vcc pin should be connected to an isolated 15V power supply. Vcc recommended limits are 14V to 16V , and shall not exceed 18V. The return of Vcc is pin 20. Recommended power supply capability is about 70mA.
20	+15V Rtn (3)	Signal ground for all signals at Pins 19 through 27. This ground is internally connected to the +VDC Rtn through 1.7 Ohms. It is preferred not to have external connection between Signal Gnd and +VDC Rtn.

Pin #	Name	Description
21	SD (3)	It is an active low, dual function input/output pin. It is internally pulled high to +5V by 2.74K Ω. As a low input it shuts down all MOSFETs regardless of the Hin and Lin signals. SD is internally activated by the over-temperature shutdown, over-current limit, and desaturation protection Desaturation shutdown is a latching feature. Over-temperature shutdown, and over-current limit are not latching features. SD can be used to shutdown all MOSFETs by an external command. An open collector switch shall be used to pull down SD externally. SD can be used as a fault condition output. Low output at SD indicates a latching fault situation.
22	Flt (3)	It is a dual function input/output pin. It is an active low input, internally pulled high to +5V by 2.74K Ω. If pulled down, it will freeze the status of all the six MOSFETs regardless of the Hin and Lin signals. As an output, Pin 13, reports desaturation protection activation. When desaturation protection is activated a low output for about 9 μsec is reported. If any other protection feature is activated, it will not be reported by Pin 22.
23	Flt-Clr (3)	is a fault clear input. It can be used to reset a latching fault condition, due to desaturation protection. Pin 23 an active high input. It is internally pulled down by 2.0KΩ. A latching fault due to desaturation can be cleared by pulling this input high to +5V by 200-500Ω, or to +15V by 3-5KΩ, as shown in Fig. 6. **It is recommended to activate fault clear input for about 300 μsec at startup.**

Pin #	Name	Description
24	+5V Output	+5V output. Maximum output current is 30mA
25	Itrip-Ref (3)	Adjustable voltage divider reference for over-current shutdown. Internal pull-up to +5V 31.6KΩ, pull down to ground is 10KΩ, and hysteresis resistance of50KΩ. The internal set point is 1.64V, corresponding to over-current shutdown of 34A. The re-start delay time is about 70 usec.
26	Idco	DC bus current sense amplifier output. The sensor gain is 0.049V/A. The internal impedance of this output is 1KΩ, and internal filter capacitance is 1nF.
27	TCo	Analog output of case temperature sensor. The sensor output gain is 0.010 V/^{o}C, with zero DC offset. This sensor can measure both positive and negative ^{o}C. The internal impedance of this output is 8.87KΩ. The internal block diagram of the temperature sensor is shown in Fig. 5.
28 &29	PhA	Phase A output
30 & 31	PhB	Phase B Output
32 & 33	PhC	Phase C Output
34 & 35	+VDC Rtn	DC Bus return
36 & 37	+VDC	DC Bus input
Case	Case	Isolated From All Terminals

Application Notes

a- Input Interface:

Recommended input turn-on current for all six drive signals is 5-8mA.
For higher noise immunity the tri-state differential buffer, DS34C87, is recommended as shown in Fig. 4.
Note : Connect LinA to non-inverting output for a non-inverting input logic.
Connect LinA to inverting output for an inverting input logic.

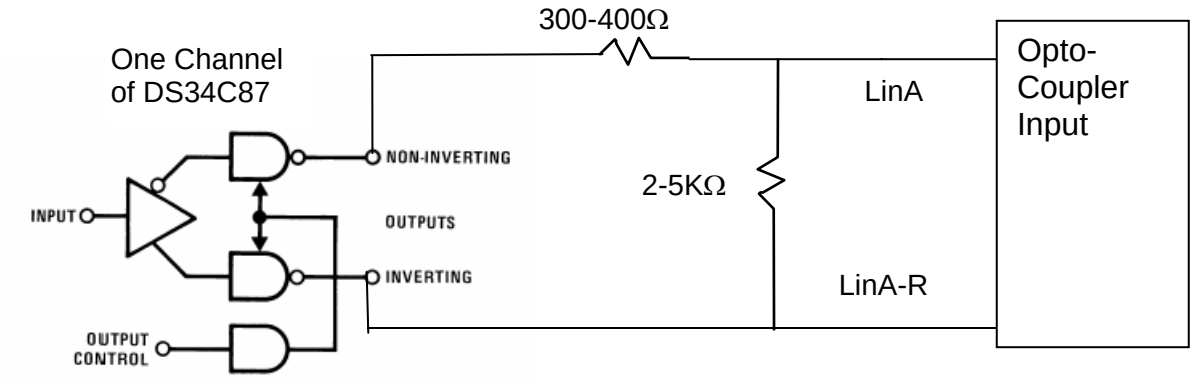


Fig. 4. Input Signal Buffer

b-Temperature Sensor Output:

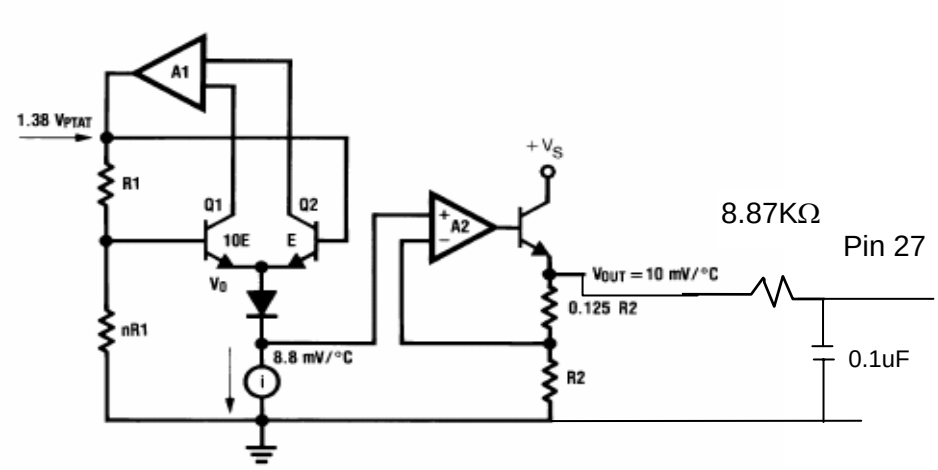


Fig. 5 Temperature Sensor Internal Block Diagram

For both negative and positive temperature measurement capability, Contact the Factory.

TECHNICAL DATA
Datasheet 4118, Rev. D.1

c- System Start Up Sequence:

Activate fault clear input for about **300 μsec** at startup. The micro-controller enable output is inverted and fed to the second DS34C87 control input. When the controller is in disable mode, the Flt-clr is enabled and Phase C low-side MOSFET is turned on. This allows for the bootstrap circuit of the high-side MOSFET of Phase C to be charged. At the same time, the high-side bootstrap circuits of Phases A and B will charge through the motor winding. Once the controller is enabled, PWM signals of all channels should start.
Fig. 6 shows a recommended startup circuit.

Notes:
1- Gnd1 and Gnd2 are isolated grounds from each other.
2- The +5V power supply used for DS34C87 is an isolated power supply.
3- The +15V power supply used for SPM6M080-010D is an isolated power supply.

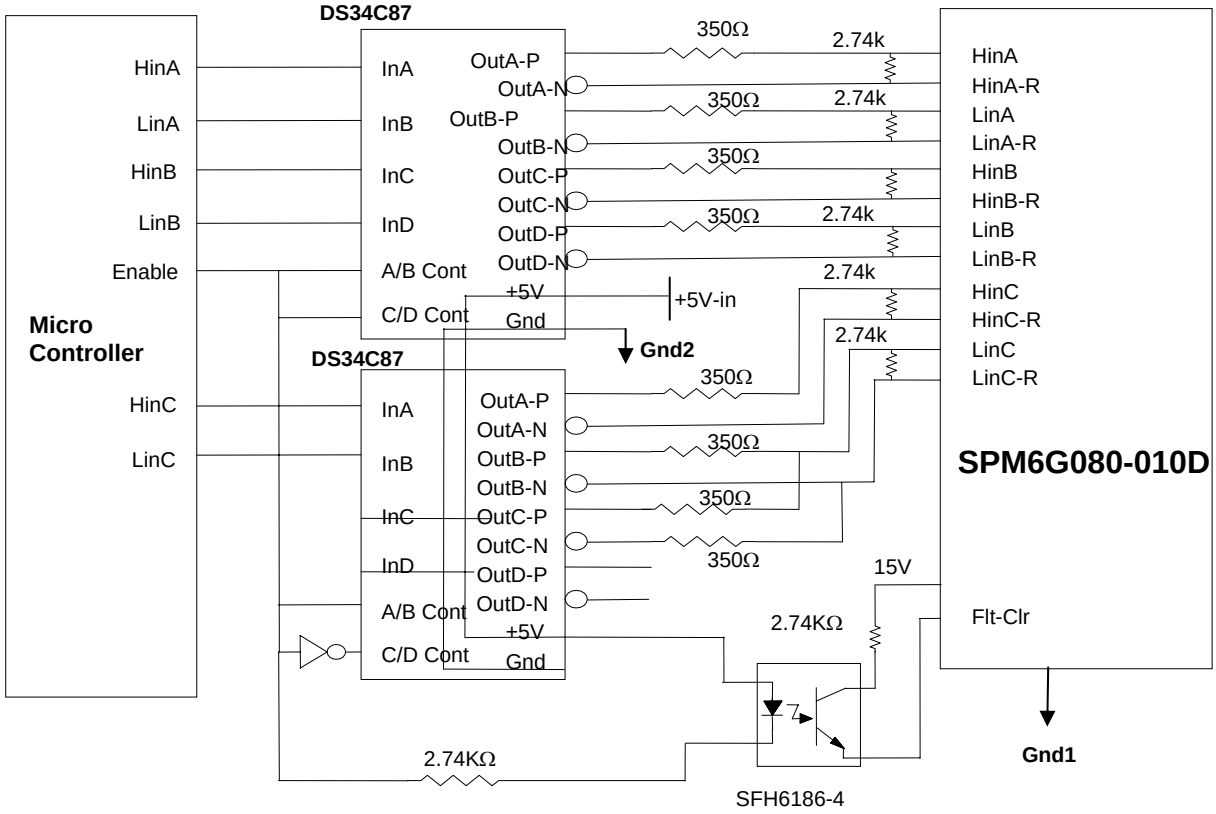


Fig. 6 Input Interface and Startup Circuit

Truth Table For DS34C87

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

d- DC Bus Charging from 15V

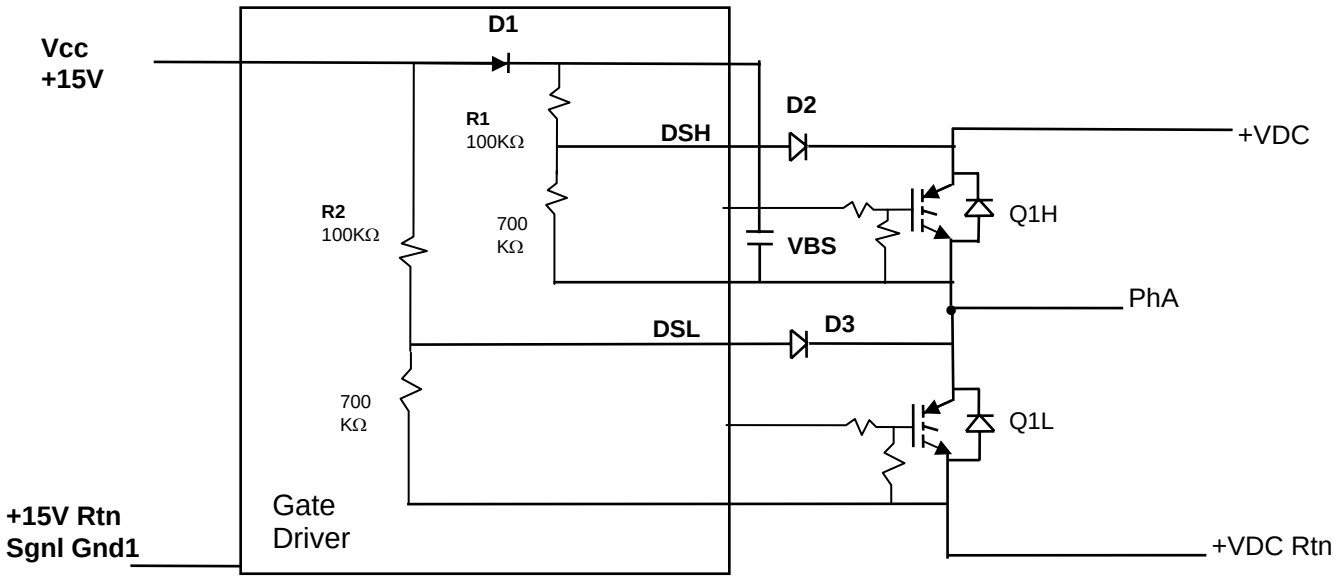


Figure 7. Charging Path from 15V Supply to DC Bus when DC Bus is off

- Each MOSFET is protected against desaturation.
- D2 is the desaturation sense diode for the high-side MOSFET
- D3 is the desaturation sense diode for the low-side MOSFET
- When the DC bus voltage is not applied or below 15V, there is a charging path from the 15V supply to the DC bus through D2 and D3 and the corresponding pull up 100K Ohm resistor. The charging current is 0.15mA per MOSFET. Total charging current is about 1.5mA.
- **Do not apply PWM signal if the DC bus voltage is below 20V.**

e- Active Bias For Desaturation Detection Circuit:

The desaturation detection is done by diode D2 for the high side MOSFET Q1H, and by diode D3 for the low side MOSFET Q1L. The internal detection circuit, input DSH for the high-side and input DSL for the low-side, is biased by the local supply voltage VCC for the low side and VBS for the high side. When the MOSFET is on the corresponding detection diode is on. The current flowing through the diode is determined by the internal pull resistor, R1 for the high side and R2 for the low side. To minimize the current drain from VCC and VBS, R1 and R2 are set to be 100KΩ. Lower value of R1 will overload the bootstrap circuit and reduce the bootstrap capacitor holding time.

To increase the circuit noise immunity, an active bias circuit is used to lower R1 and R2 when the corresponding MOSFET is off by monitoring the input voltage at both DSH, DSL inputs. If the inputs at DSH drops below 7V the active bias is disabled. The active bias circuits result in reducing R1 or R2 to about 110 Ω when the corresponding input is above 8V, as shown in Fig. 8. This active circuit results in higher noise immunity.

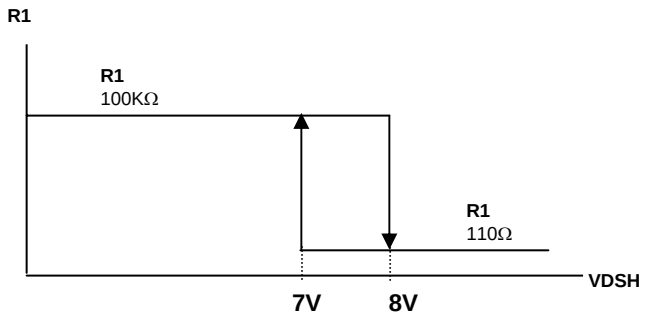


Figure 8. Active Bias for DSH and DSL Internal Inputs

f- Limitation With Trapezoidal Motor Drive

In trapezoidal motor drives, two phases are conducting while the third phase is off at any time. In Fig. 9 shows the voltage waveform across one phase, during intervals t1 and t2, the MOSFET is off while the active bias circuit is above 8V, and below 15V. This results in activating the active pull up circuit and reducing the corresponding R1 or R2 down to about 110 Ω. A high current will flow from VCC or VBS through R2 or R1 and the motor winding during intervals t1, and t2. This results in draining the bootstrap capacitor voltage quickly.

Contact the factory for adjustments to satisfy trapezoidal motor drive applications using this module. The adjustment will disable the internal pull up circuit.

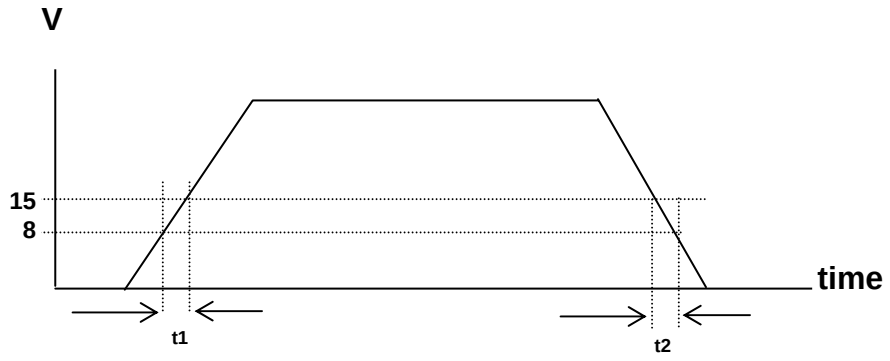


Figure 9. Active Bias for DSH and DSL Internal Inputs

Cleaning Process:
Suggested precaution following cleaning procedure:
If the parts are to be cleaned in an aqueous based cleaning solution, it is recommended that the parts be baked immediately after cleaning. This is to remove any moisture that may have permeated into the device during the cleaning process. For aqueous based solutions, the recommended process is to bake for at least 2 hours at 125^{o}C.
Do not use solvents based cleaners.

Soldering Procedure:
Recommended soldering procedure
Signal pins 1 to 27: 210C for 10 seconds max
Power pins 28 to 37: 260C for 10 seconds max. Pre-warm module to 125C to aid in power pins soldering.

Ordering Information:
SPM6M080-010D comes standard with a uni-directional current sense signal. For optional bi-directional current sense signal, add –A to the part number as follows: SPM6M080-010D-A.